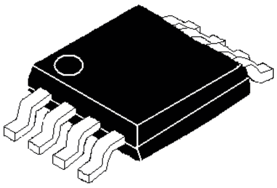
# TSB572

## Low-power, 2.5 MHz, RR IO, 36 V BiCMOS operational amplifier

Datasheet - production data



MiniSO8

DFN8 3x3

## Features

- Low-power consumption: 380 µA typ
- Wide supply voltage: 4 V - 36 V
- Rail-to-rail input and output
- Gain bandwidth product: 2.5 MHz
- Low input bias current: 30 nA max
- No phase reversal
- High tolerance to ESD: 4 kV HBM
- Extended temperature range: -40 °C to 125 °C
- Automotive grade
- Small SMD packages
- 40 V BiCMOS technology
- Enhanced stability vs. capacitive load

## Applications

- Active filtering
- Audio systems
- Automotive
- Power supplies
- Industrial
- Low/High side current sensing

## Description

The TSB572 dual operational amplifier offers extended voltage operating range from 4 V to 36 V and rail-to-rail input/output.

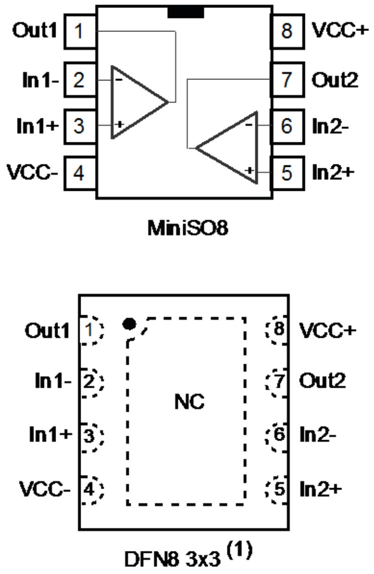
The TSB572 offers a very good speed/power consumption ratio with 2.5 MHz gain bandwidth product while consuming only 380 µA typically at 36 V supply voltage.

Stability and robustness of the TSB572 make it an ideal solution for a wide voltage range of applications.

# Contents

# 1 Package pin connections

**Figure 1: Pin connections for each package (top view)**



1. Exposed pad can be left floating or connected to ground

# 2 Absolute maximum ratings and operating conditions

**Table 1: Absolute maximum ratings**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage (1) | | 40 | V |
| $V_{id}$ | Differential input voltage (2) | | ±1 | |
| $V_{in}$ | Input voltage (3) | | $(V_{CC}^-) - 0.2$ to $(V_{CC}^+) + 0.2$ | |
| $I_{in}$ | Input current (4) | | 10 | mA |
| $T_{stg}$ | Storage temperature | | -65 to 150 | °C |
| $T_j$ | Maximum junction temperature | | 150 | |
| $R_{thja}$ | Thermal resistance junction to ambient (5)(6) | MiniSO8 | 190 | °C/W |
| | | DFN8 3x3 | 40 | |
| ESD | Human body model (HBM) (7) | | 4 | kV |
| | Machine model (MM) (8) | | 100 | V |
| | CDM: charged device model (9) | | 1.5 | kV |
| | Latch-up immunity | | 200 | mA |

**Notes:**

(1)All voltage values, except the differential voltage are with respect to network ground terminal.

(2)Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.

(3)$V_{CC}$-$V_{in}$ must not exceed 6 V, Vin must not exceed 6 V.

(4)Input current must be limited by a resistor in-series with the inputs.

(5)$R_{th}$ are typical values.

(6)Short-circuits can cause excessive heating and destructive dissipation.

(7)According to JEDEC standard JESD22-A114F.

(8)According to JEDEC standard JESD22-A115A.

(9)According to ANSI/ESD STM5.3.1.

**Table 2: Operating conditions**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4 to 36 | V |
| $V_{icm}$ | Common mode input voltage range | $(V_{CC}^-) - 0.1$ to $(V_{CC}^+) + 0.1$ | |
| $T_{oper}$ | Operating free-air temperature range | -40 to 125 | °C |

# 3 Electrical characteristics

**Table 3: Electrical characteristics at Vcc = 4 V, Vicm = Vcc/2, Tamb = 25 °C, and RL connected to Vcc/2 (unless otherwise specified)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **DC performance** | | | | | | |
| $V_{io}$ | Input offset voltage | | -1.5 | | 1.5 | mV |
| | | -40 °C < T < 125 °C | -2.1 | | 2.1 | |
| $\Delta V_{io}/\Delta T$ | Input offset voltage drift | -40 °C < T < 125 °C | | 1.5 | 6 | µV/°C |
| $I_{io}$ | Input offset current | | | 2 | 15 | nA |
| | | -40 °C < T < 125 °C | | | 35 | |
| $I_{ib}$ | Input bias current | | | 8 | 30 | |
| | | -40 °C < T < 125 °C | | | 70 | |
| $C_{IN}$ | Input capacitor | | | 2 | | pF |
| $R_{IN}$ | Input impedance | | | 1 | | TΩ |
| CMR | Common mode rejection ratio 20 log ($\Delta V_{icm}/\Delta V_{io}$) | $V_{icm}$ = ($V_{CC-}$) to ($V_{CC+}$) - 1.5 V, $V_{out}$ = $V_{CC}/2$ | 90 | 114 | | dB |
| | | -40 °C < T < 125 °C | 80 | | | |
| | | $V_{icm}$ = ($V_{CC-}$) to ($V_{CC+}$), $V_{out}$ = $V_{CC}/2$ | 75 | 97 | | |
| | | -40 °C < T < 125 °C | 70 | | | |
| $A_{vd}$ | Large signal voltage gain | $R_L$= 10 kΩ, $V_{out}$ = 0.5 to 3.5 V | 90 | 100 | | |
| | | -40 °C < T < 125 °C | 85 | | | |
| $V_{OH}$ | High level output voltage (drop voltage from ($V_{CC+}$)) | $R_L$ = 10 kΩ | | 19 | 60 | mV |
| | | -40 °C < T < 125 °C | | | 80 | |
| $V_{OL}$ | Low level output voltage | $R_L$ = 10 kΩ | | 12 | 50 | |
| | | -40 °C < T < 125 °C | | | 70 | |
| $I_{out}$ | $I_{sink}$ | $V_{out}$ = $V_{CC}$ | 20 | 38 | | mA |
| | | -40 °C < T < 125 °C | 5 | | | |
| | $I_{source}$ | $V_{out}$ = 0 V | 10 | 32 | | |
| | | -40 °C < T < 125 °C | 5 | | | |
| $I_{CC}$ | Supply current (per channel) | No load, $V_{out}$ = $V_{CC}/2$ | | 340 | 430 | µA |
| | | -40 °C < T < 125 °C | | | 500 | |
| **AC performance** | | | | | | |
| GBP | Gain bandwidth product | $R_L$ = 10 kΩ, $C_L$ = 100 pF | 1.5 | 2.2 | | MHz |
| | | -40 °C < T < 125 °C | 1.2 | | | |
| $\phi_m$ | Phase margin | $R_L$ = 10 kΩ, $C_L$ = 100 pF | | 45 | | degrees |
| $G_m$ | Gain margin | $R_L$ = 10 kΩ, $C_L$ = 100 pF | | 5 | | dB |

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| SR | Negative slew rate | $V_{in}$ = 3.5 to 0.5 V, $A_v$ = 1, 10 % to 90 %, $R_L$ = 10 kΩ, $C_L$ = 100 pF | 0.50 | 0.78 | | V/µs |
| | | -40 °C < T < 125 °C | 0.37 | | | |
| | Positive slew rate | $V_{in}$ = 0.5 to 3.5 V, $A_v$ = 1, 10 % to 90 %, $R_L$ = 10 kΩ, $C_L$ = 100 pF | 0.50 | 0.89 | | |
| | | -40 °C < T < 125 °C | 0.37 | | | |
| $e_n$ | Equivalent input noise voltage | f = 1 kHz | | 20 | | nV/√Hz |
| | | f = 0.1 Hz to 10 Hz | | 0.7 | | µVpp |
| THD+N | Total harmonic distortion + noise | f = 1 kHz, $V_{in}$ = 3.8 $V_{pp}$, $R_L$ = 10 kΩ, $C_L$ = 100 pF | | 0.001 | | % |

**Table 4: Electrical characteristics at Vcc = 12 V, Vicm = Vcc/2, Tamb = 25 °C, and RL connected to Vcc/2 (unless otherwise specified)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **DC performance** | | | | | | |
| $V_{io}$ | Input offset voltage | | -1.5 | | 1.5 | mV |
| | | -40 °C < T < 125 °C | -2.1 | | 2.1 | |
| $\Delta V_{io}/\Delta T$ | Input offset voltage drift | -40 °C < T < 125 °C | | 1.5 | 6 | μV/°C |
| $I_{io}$ | Input offset current | | | 2 | 15 | nA |
| | | -40 °C < T < 125 °C | | | 35 | |
| $I_{ib}$ | Input bias current | | | 8 | 30 | |
| | | -40 °C < T < 125 °C | | | 70 | |
| $C_{IN}$ | Input capacitor | | | 2 | | pF |
| $R_{IN}$ | Input impedance | | | 1 | | TΩ |
| CMR | Common mode rejection ratio 20 log ($\Delta V_{icm}/\Delta V_{io}$) | $V_{icm}$ = ($V_{CC-}$) to ($V_{CC+}$) - 1.5 V, $V_{out} = V_{CC}/2$ | 100 | 123 | | dB |
| | | -40 °C < T < 125 °C | 90 | | | |
| | | $V_{icm}$ = ($V_{CC-}$) to ($V_{CC+}$), $V_{out} = V_{CC}/2$ | 85 | 106 | | |
| | | -40 °C < T < 125 °C | 80 | | | |
| SVR | Supply voltage rejection ratio 20 log ($\Delta V_{CC}/\Delta V_{io}$) | $V_{CC}$ = 4 to 12 V | 90 | 99 | | |
| | | -40 °C < T < 125 °C | 80 | | | |
| $A_{vd}$ | Large signal voltage gain | $R_L$= 10 kΩ, $V_{out}$ = 0.5 to 11.5 V | 95 | 106 | | |
| | | -40 °C < T < 125 °C | 90 | | | |
| $V_{OH}$ | High level output voltage (drop voltage from $V_{CC+}$) | $R_L$ = 10 kΩ | | 38 | 100 | mV |
| | | -40 °C < T < 125 °C | | | 150 | |
| $V_{OL}$ | Low level output voltage | $R_L$ = 10 kΩ | | 16 | 70 | |
| | | -40 °C < T < 125 °C | | | 90 | |
| $I_{out}$ | $I_{sink}$ | $V_{out} = V_{CC}$ | 20 | 42 | | mA |
| | | -40 °C < T < 125 °C | 8 | | | |
| | $I_{source}$ | $V_{out}$ = 0 V | 15 | 35 | | |
| | | -40 °C < T < 125 °C | 7 | | | |
| $I_{CC}$ | Supply current (per channel) | No load, $V_{out} = V_{CC}/2$ | | 360 | 450 | μA |
| | | -40 °C < T < 125 °C | | | 530 | |
| **AC performance** | | | | | | |
| GBP | Gain bandwidth product | $R_L$ = 10 kΩ, $C_L$ = 100 pF | 1.6 | 2.4 | | MHz |
| | | -40 °C < T < 125 °C | 1.3 | | | |
| $\phi_m$ | Phase margin | $R_L$ = 10 kΩ, $C_L$ = 100 pF | | 50 | | degrees |
| $G_m$ | Gain margin | $R_L$ = 10 kΩ, $C_L$ = 100 pF | | 6 | | dB |

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| SR | Negative slew rate | $V_{in}$ = 10.5 to 1.5 V, $A_v$ = 1, 10 % to 90 %, $R_L$ = 10 kΩ, $C_L$ = 100 pF | 0.53 | 0.82 | | V/µs |
| | | -40 °C < T < 125 °C | 0.40 | | | |
| | Positive slew rate | $V_{in}$ = 1.5 to 10.5 V, $A_v$ = 1, 10 % to 90 %, $R_L$ = 10 kΩ, $C_L$ = 100 pF | 0.55 | 0.92 | | |
| | | -40 °C < T < 125 °C | 0.40 | | | |
| $e_n$ | Equivalent input noise voltage | f = 1 kHz | | 20 | | nV/√Hz |
| | | f = 0.1 Hz to 10 Hz | | 0.7 | | µVpp |
| THD+N | Total harmonic distortion + noise | f = 1 kHz, $V_{in}$ = 7 $V_{pp}$, $R_L$ = 10 kΩ, $C_L$ = 100 pF | | 0.0005 | | % |

**Table 5: Electrical characteristics at Vcc = 36 V, Vicm = Vcc/2, Tamb = 25 °C, and RL connected to Vcc/2 (unless otherwise specified)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **DC performance** | | | | | | |
| $V_{io}$ | Input offset voltage | | -1.5 | | 1.5 | mV |
| | | -40 °C < T < 125 °C | -2.1 | | 2.1 | |
| $\Delta V_{io}/\Delta T$ | Input offset voltage drift | -40 °C < T < 125 °C | | 1.5 | 6 | µV/°C |
| $\Delta V_{io}$ | Long-term input offset voltage drift (1) | T = 25 °C | | 1.5 | | µV/√month |
| $I_{io}$ | Input offset current | | | 2 | 15 | nA |
| | | -40 °C < T < 125 °C | | | 35 | |
| $I_{ib}$ | Input bias current | | | 8 | 30 | |
| | | -40 °C < T < 125 °C | | | 70 | |
| $C_{IN}$ | Input capacitor | | | 2 | | pF |
| $R_{IN}$ | Input impedance | | | 1 | | TΩ |
| CMR | Common mode rejection ratio 20 log ($\Delta V_{icm}/\Delta V_{io}$) | $V_{icm}$ = ($V_{CC-}$) to ($V_{CC+}$) - 1.5 V, $V_{out}$ = $V_{CC}/2$ | 105 | 129 | | dB |
| | | -40 °C < T < 125 °C | 95 | | | |
| | | $V_{icm}$ = ($V_{CC-}$) to ($V_{CC+}$), $V_{out}$ = $V_{CC}/2$ | 95 | 115 | | |
| | | -40 °C < T < 125 °C | 90 | | | |
| SVR | Supply voltage rejection ratio 20 log ($\Delta V_{CC}/\Delta V_{io}$) | $V_{CC}$ = 4 to 36 V | 90 | 104 | | |
| | | -40 °C < T < 125 °C | 85 | | | |
| $A_{vd}$ | Large signal voltage gain | $R_L$= 10 kΩ, $V_{out}$ = 0.5 to 35.5 V | 95 | 114 | | |
| | | -40 °C < T < 125 °C | 90 | | | |
| $V_{OH}$ | High level output voltage (drop voltage from $V_{CC+}$) | $R_L$ = 10 kΩ | | 78 | 150 | mV |
| | | -40 °C < T < 125 °C | | | 200 | |
| $V_{OL}$ | Low level output voltage | $R_L$ = 10 kΩ | | 30 | 90 | |
| | | -40 °C < T < 125 °C | | | 120 | |
| $I_{out}$ | $I_{sink}$ | $V_{out}$ = $V_{CC}$ | 25 | 65 | | mA |
| | | -40 °C < T < 125 °C | 10 | | | |
| | $I_{source}$ | $V_{out}$ = 0 V | 20 | 50 | | |
| | | -40 °C < T < 125 °C | 10 | | | |
| $I_{CC}$ | Supply current (per channel) | No load, $V_{out}$ = $V_{CC}/2$ | | 380 | 470 | µA |
| | | -40 °C < T < 125 °C | | | 550 | |
| **AC performance** | | | | | | |
| GBP | Gain bandwidth product | $R_L$ = 10 kΩ, $C_L$ = 100 pF | 1.7 | 2.5 | | MHz |
| | | -40 °C < T < 125 °C | 1.4 | | | |
| $\phi_m$ | Phase margin | $R_L$ = 10 kΩ, $C_L$ = 100 pF | | 50 | | degrees |
| $G_m$ | Gain margin | $R_L$ = 10 kΩ, $C_L$ = 100 pF | | 8 | | dB |

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| SR | Negative slew rate | $V_{in}$ = 22.5 to 13.5 V, $A_v$ = 1, 10 % to 90 %, $R_L$ = 10 kΩ, $C_L$ = 100 pF | 0.57 | 0.88 |  | V/µs |
|  |  | -40 °C < T < 125 °C | 0.44 |  |  |  |
|  | Positive slew rate | $V_{in}$ = 13.5 to 22.5 V, $A_v$ = 1, 10 % to 90 %, $R_L$ = 10 kΩ, $C_L$ = 100 pF | 0.60 | 1.00 |  |  |
|  |  | -40 °C < T < 125 °C | 0.44 |  |  |  |
| $e_n$ | Equivalent input noise voltage | f = 1 kHz |  | 20 |  | nV/√Hz |
|  |  | f = 0.1 Hz to 10 Hz |  | 0.7 |  | µVpp |
| THD+N | Total harmonic distortion + noise | f = 1 kHz, $V_{in}$ = 7 $V_{pp}$, $R_L$ = 10 kΩ, $C_L$ = 100 pF |  | 0.001 |  | % |

**Notes:**

(1)Typical value is based on the $V_{io}$ drift observed after 1000h at 125 °C extrapolated to 25 °C using Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration (see *Section 4.5*).

Figure 2: Supply current vs. supply voltage

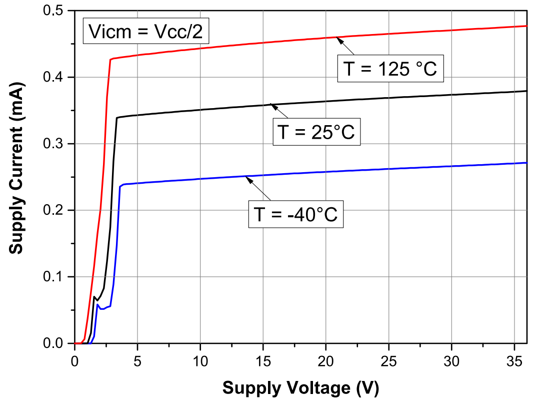


Figure 3: Input offset voltage distribution at VCC = 4 V

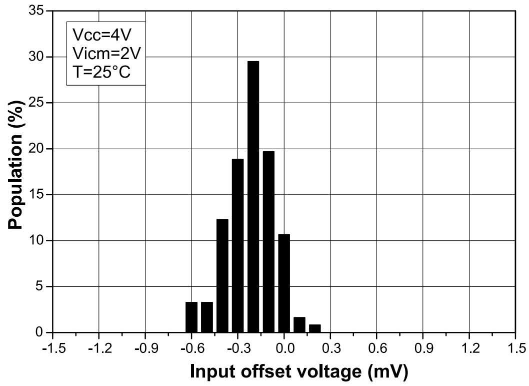


Figure 4: Input offset voltage distribution at VCC = 12 V

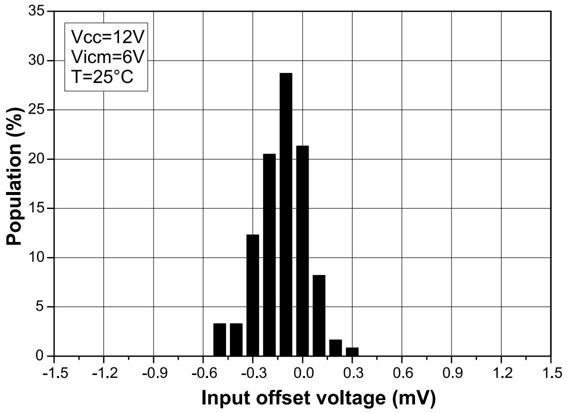


Figure 5: Input offset voltage distribution at VCC = 36 V

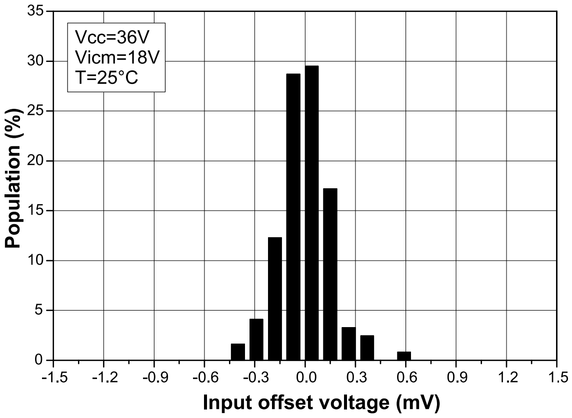


Figure 6: Input offset voltage vs. temperature at VCC = 36 V

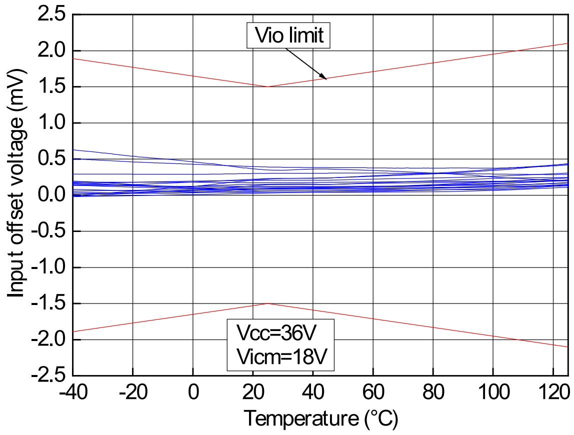


Figure 7: Input offset voltage temperature variation distribution at VCC = 36 V

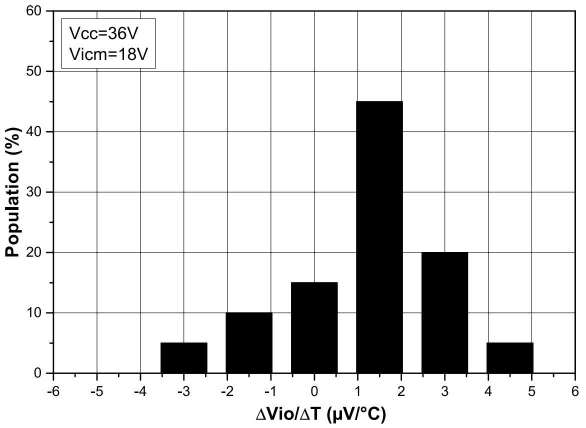


Figure 8: Input offset voltage vs. supply voltage

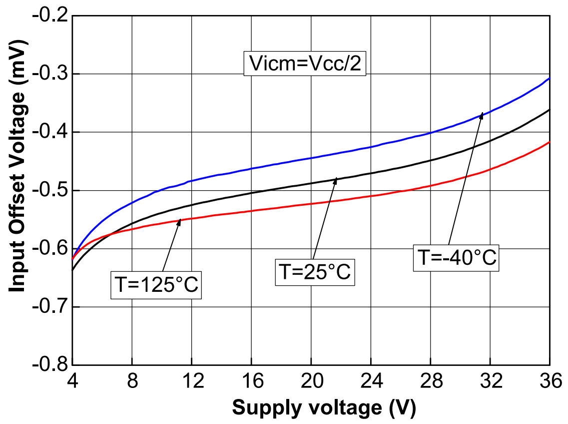


Figure 9: Input offset voltage vs. common-mode voltage at VCC = 4 V

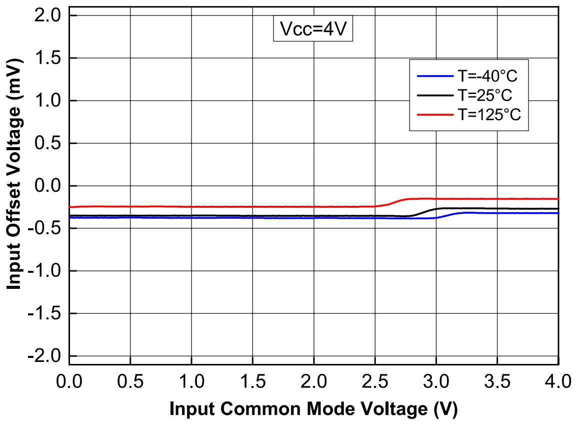


Figure 10: Input offset voltage vs. common-mode voltage at VCC = 36 V

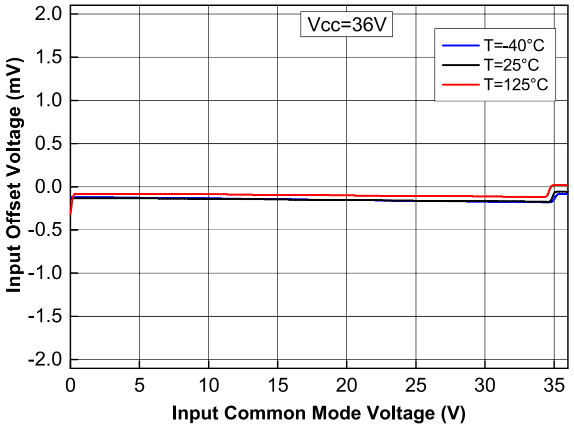


Figure 11: Input bias current vs. temperature at VICM = VCC/2

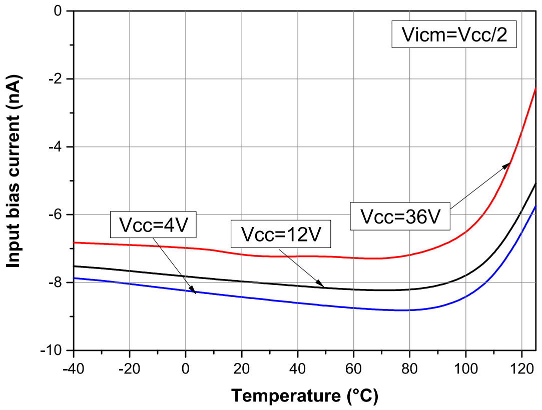


Figure 12: Input bias current vs. common-mode voltage at VCC = 36 V

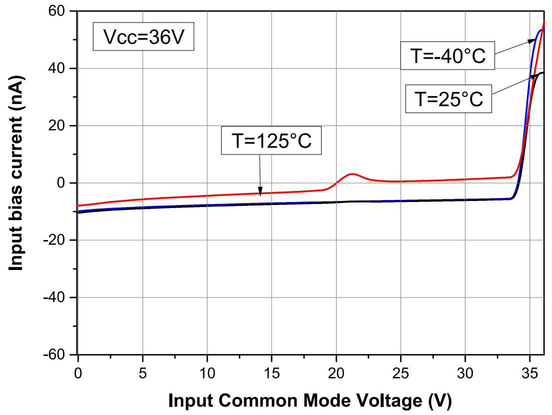


Figure 13: Output current vs. output voltage at VCC = 4 V

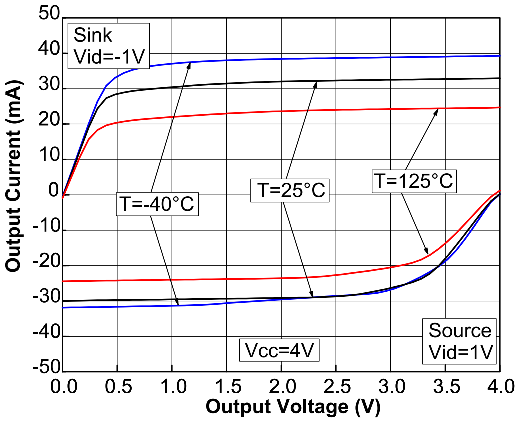


Figure 14: Output current vs. output voltage at VCC = 36 V

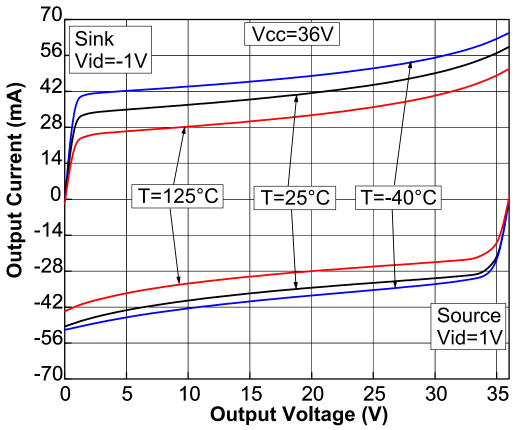


Figure 15: Output voltage (Voh) vs. supply voltage

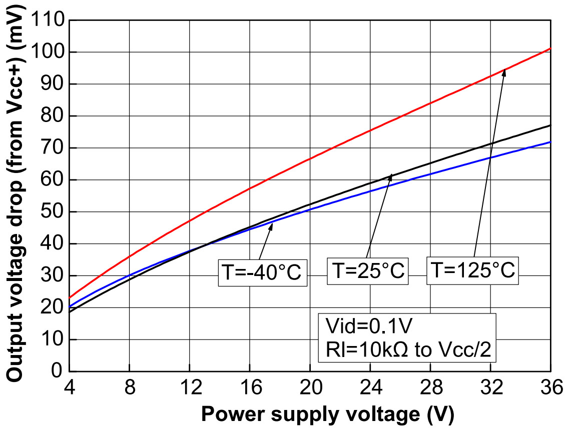


Figure 16: Output voltage (Vol) vs. supply voltage

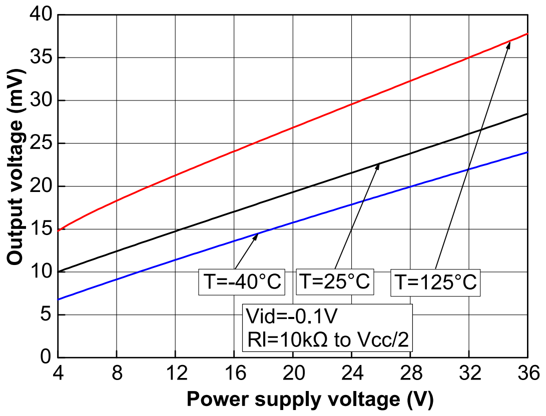


Figure 17: Negative slew rate at VCC = 36 V

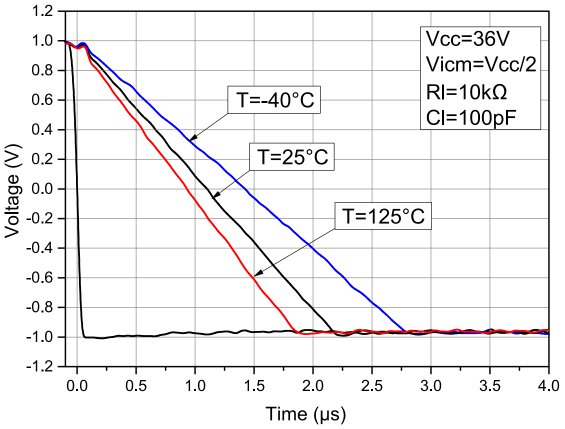


Figure 18: Positive slew rate at VCC = 36 V

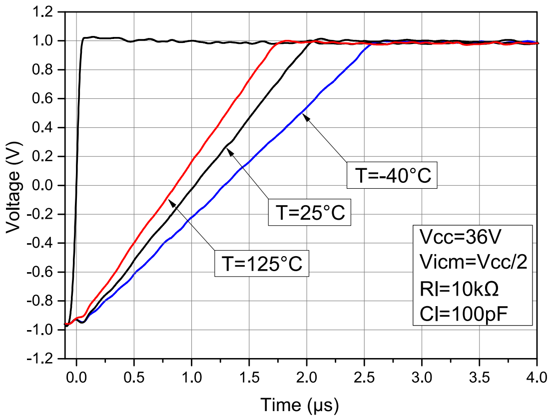


Figure 19: Slew rate vs. supply voltage

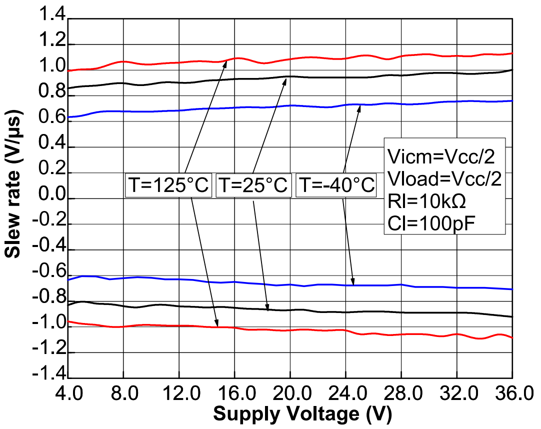


Figure 20: Bode diagram at VCC = 4 V

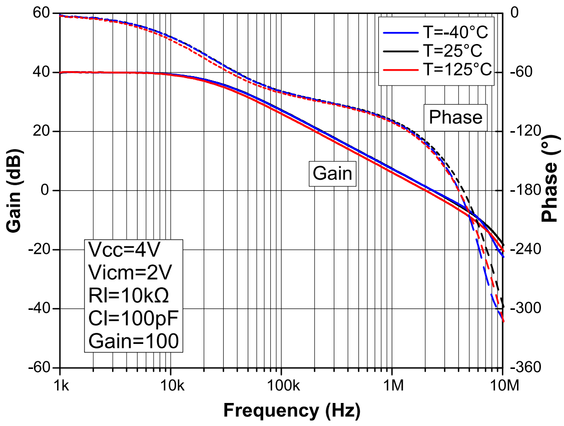


Figure 21: Bode diagram at VCC = 36 V

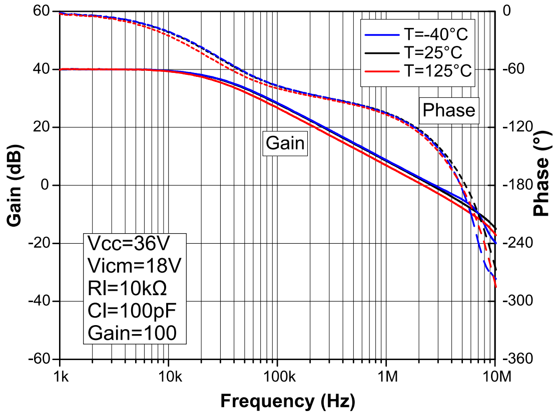


Figure 22: Phase margin vs. output current at VCC = 4 V

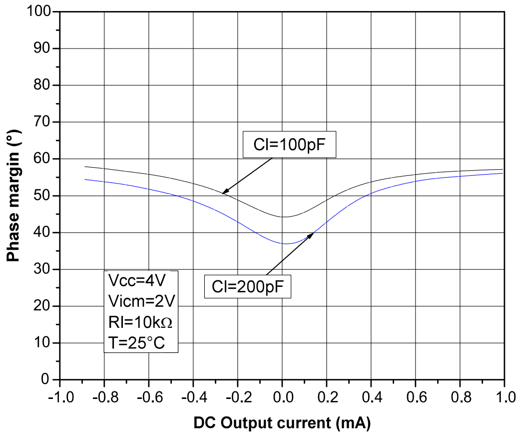


Figure 23: Phase margin vs. output current at VCC = 36 V

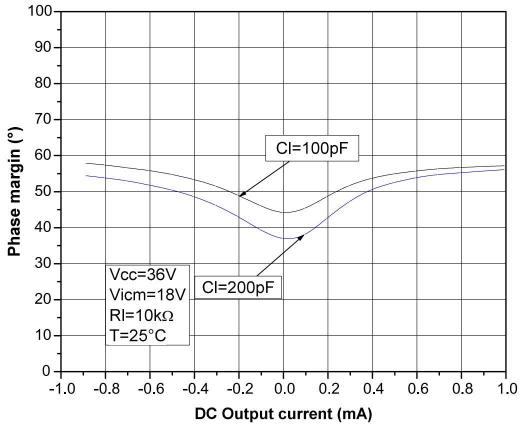


Figure 24: Phase margin vs. capacitive load

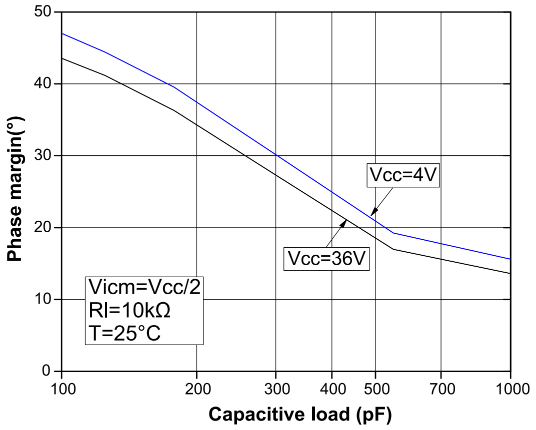


Figure 25: Overshoot vs. capacitive load at VCC = 36 V

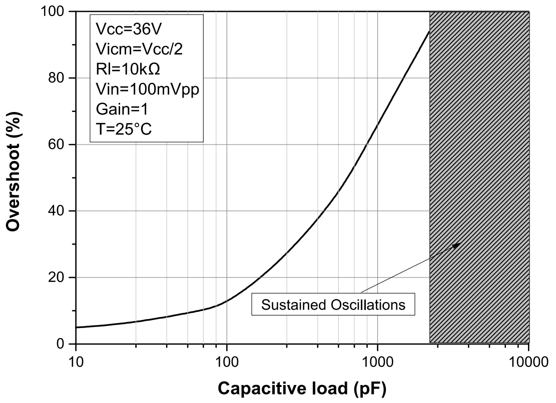


Figure 26: Small step response vs. time at VCC = 4 V

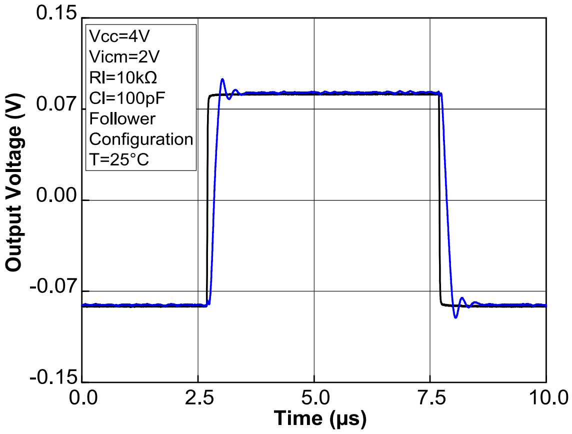


Figure 27: Output desaturation vs. time

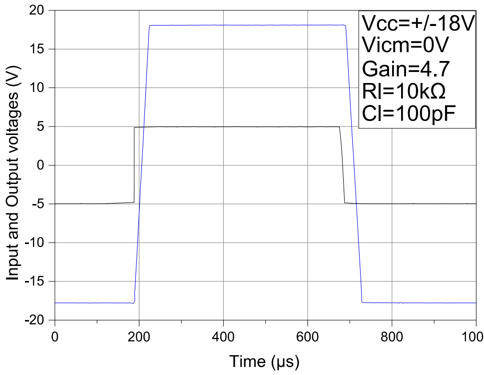


Figure 28: Amplifier behavior close to the rails at VCC = 36 V

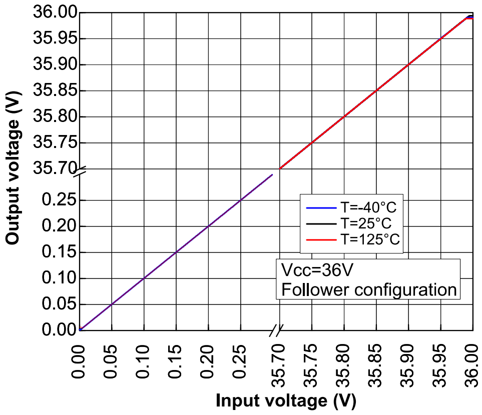


Figure 29: Noise vs. frequency at VCC = 36 V

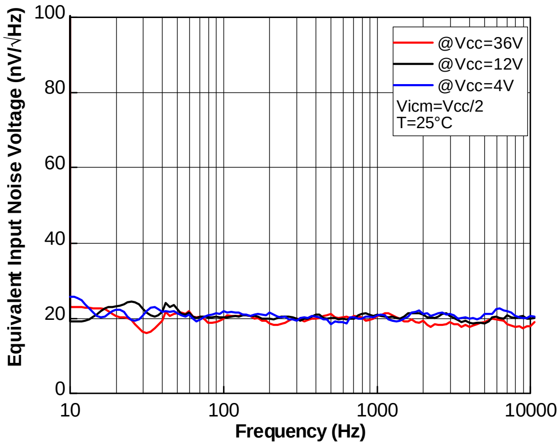


Figure 30: Noise vs. time at VCC = 36 V

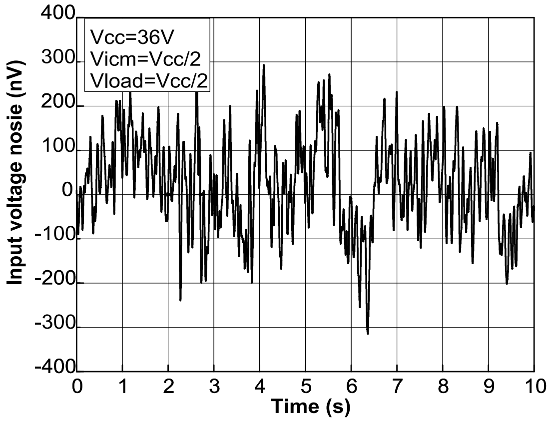


Figure 31: THD+N vs. frequency

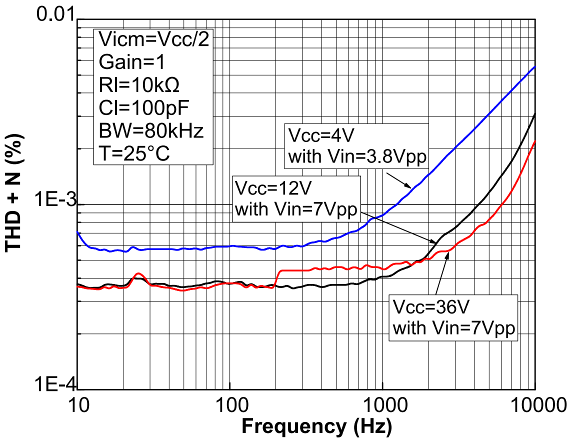


Figure 32: THD+N vs. output voltage

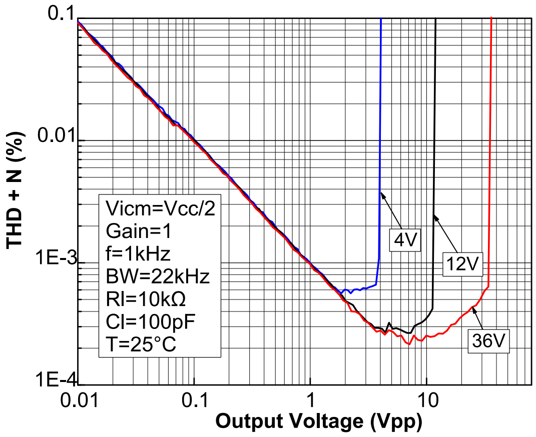


Figure 33: PSRR vs. frequency at VCC = 36 V

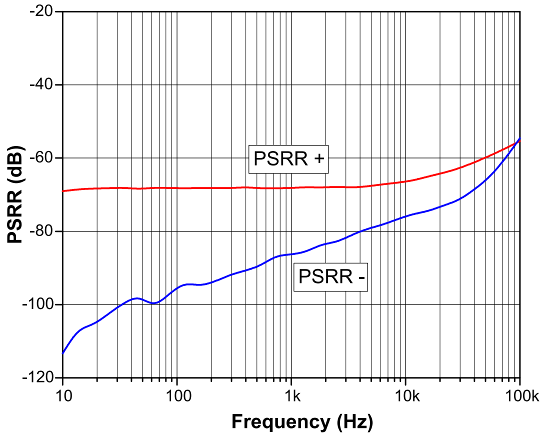
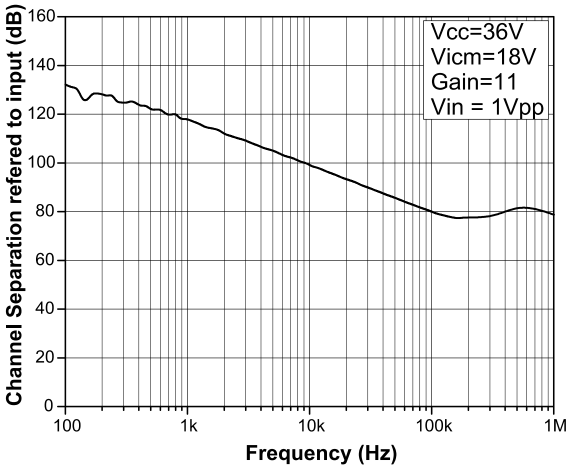


Figure 34: Channel separation vs. frequency at VCC= 36 V



# 4 Application information

## 4.1 Operating voltages

The TSB572 can operate from 4 V to 36 V. The parameters are fully specified for 4 V, 12 V, and 36 V power supplies. However, the parameters are stable in the full $V_{CC}$ range. Additionally, the main specifications are guaranteed in extended temperature ranges from -40 to 125 °C.

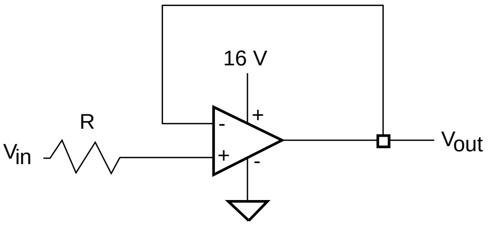
## 4.2 Input pin voltage ranges

The TSB572 has internal ESD diode protection on the inputs. These diodes are connected between the inputs and each supply rail to protect the input transistors from electrical discharge.

If the input pin voltage exceeds the power supply by 0.2 V, the ESD diodes become conductive and excessive current can flow through them. Without limitation this over current can damage the device.

In this case, it is important to limit the current to 10 mA, by adding resistance on the input pin, as shown in *Figure 35: "Input current limitation"*.

**Figure 35: Input current limitation**



## 4.3 Rail-to-rail input

The TSB572 has rail-to-rail inputs. The input common mode range is extended from $(V_{CC-}) - 0.1$ V to $(V_{CC+}) + 0.1$ V at T = 25 °C.

## 4.4 Input offset voltage drift over temperature

The maximum input voltage drift variation over temperature is defined as the offset variation related to the offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift over temperature enables the system designer to anticipate the effect of temperature variations.

The maximum input voltage drift over temperature is computed using *Equation 1*.

**Equation 1**

$$\frac{\Delta V_{io}}{\Delta T} = \max\left|\frac{V_{io}(T) - V_{io}(25\,°C)}{T - 25\,°C}\right|$$

where T = -40 °C and 125 °C.

The TSB572 datasheet maximum value is guaranteed by measurements on a representative sample size ensuring a $C_{pk}$ (process capability index) greater than 1.3.

## 4.5 Long term input offset voltage drift

To evaluate product reliability, two types of stress acceleration are used:

- Voltage acceleration, by changing the applied voltage
- Temperature acceleration, by changing the die temperature (below the maximum junction temperature allowed by the technology) with the ambient temperature.

The voltage acceleration has been defined based on JEDEC results, and is defined using *Equation 2*.

**Equation 2**

$$A_{FV} = e^{\beta \cdot (V_S - V_U)}$$

Where:

$A_{FV}$ is the voltage acceleration factor

$\beta$ is the voltage acceleration constant in 1/V, constant technology parameter ($\beta = 1$)

$V_S$ is the stress voltage used for the accelerated test

$V_U$ is the voltage used for the application

The temperature acceleration is driven by the Arrhenius model, and is defined in *Equation 3*.

**Equation 3**

$$A_{FT} = e^{\frac{E_a}{k} \cdot \left(\frac{1}{T_U} - \frac{1}{T_S}\right)}$$

Where:

$A_{FT}$ is the temperature acceleration factor

$E_a$ is the activation energy of the technology based on the failure rate k is the Boltzmann constant ($8.6173 \times 10^{-5}$ eV.K$^{-1}$)

$T_U$ is the temperature of the die when $V_U$ is used (K)

$T_S$ is the temperature of the die under temperature stress (K)

The final acceleration factor, $A_F$, is the multiplication of the voltage acceleration factor and the temperature acceleration factor (*Equation 4*).

**Equation 4**

$$A_F = A_{FT} \times A_{FV}$$

$A_F$ is calculated using the temperature and voltage defined in the mission profile of the product. The $A_F$ value can then be used in *Equation 5* to calculate the number of months of use equivalent to 1000 hours of reliable stress duration.

**Equation 5**

$$\text{Months} = A_F \times 1000\text{ h} \times 12\text{ months} / (24\text{ h} \times 365.25\text{ days})$$

To evaluate the op amp reliability, a follower stress condition is used where $V_{CC}$ is defined as a function of the maximum operating voltage and the absolute maximum rating (as recommended by JEDEC rules).

The $V_{io}$ drift (in µV) of the product after 1000 h of stress is tracked with parameters at different measurement conditions (see *Equation 6*).

**Equation 6**

$$V_{CC} = \text{max}V_{op}\text{ with }V_{icm} = V_{CC}/2$$

The long term drift parameter ($\Delta V_{io}$), estimating the reliability performance of the product, is obtained using the ratio of the $V_{io}$ (input offset voltage value) drift over the square root of the calculated number of months (*Equation 7*).

**Equation 7**

$$\Delta V_{io} = \frac{V_{io}\text{drift}}{\sqrt{(\text{months})}}$$

Where $V_{io}$ drift is the measured drift value in the specified test conditions after 1000 h stress duration.

## 4.6 Capacitive load

Driving large capacitive loads can cause stability problems. Increasing the load capacitance produces gain peaking in the frequency response, with overshoot and ringing in the step response. It is usually considered that with a gain peaking higher than 2.3 dB an op amp might become unstable.

Generally, unity gain configuration is the worst situation for stability and the ability to drive large capacitive loads.

*Figure 36: "Stability criteria with a serial resistor at different supply voltages"* shows the serial resistor that must be added to the output, to make a system stable. *Figure 37: "Test configuration for Riso"* shows the test configuration using an isolation resistor, Riso.

**Figure 36: Stability criteria with a serial resistor at different supply voltages**

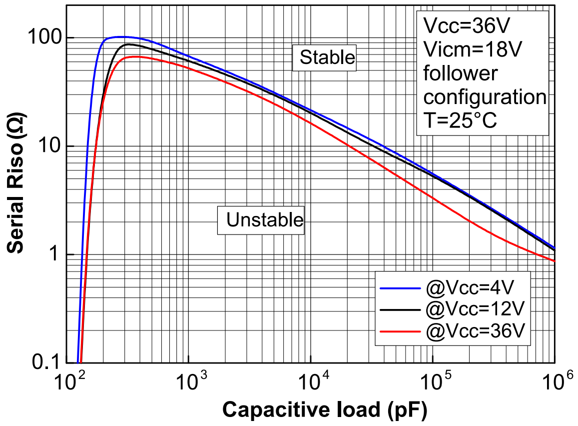
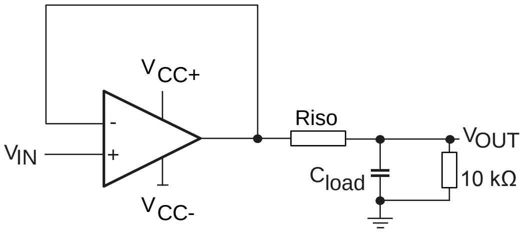


**Figure 37: Test configuration for Riso**



## 4.7 PCB layout recommendations

Particular attention must be paid to the layout of the PCB tracks connected to the amplifier, load, and power supply. The power and ground traces are critical as they must provide adequate energy and grounding for all circuits. The best practice is to use short and wide PCB traces to minimize voltage drops and parasitic inductance.

In addition, to minimizing parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used.

The copper traces that connect the output pins to the load and supply pins should be as wide as possible to minimize trace resistance.

## 4.8 Optimized application recommendation

It is recommended to place a 22 nF capacitor as close as possible to the supply pin. A good decoupling will help to reduce electromagnetic interference impact.

# 5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

## 5.1 MiniSO8 package information

**Figure 38: MiniSO8 package outline**

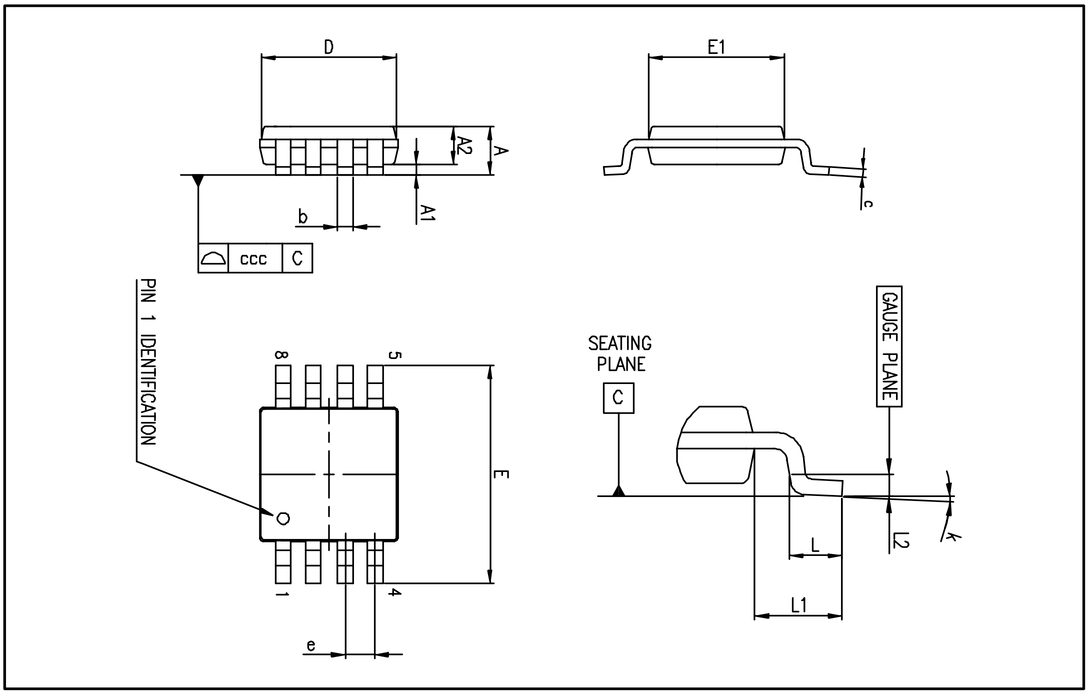
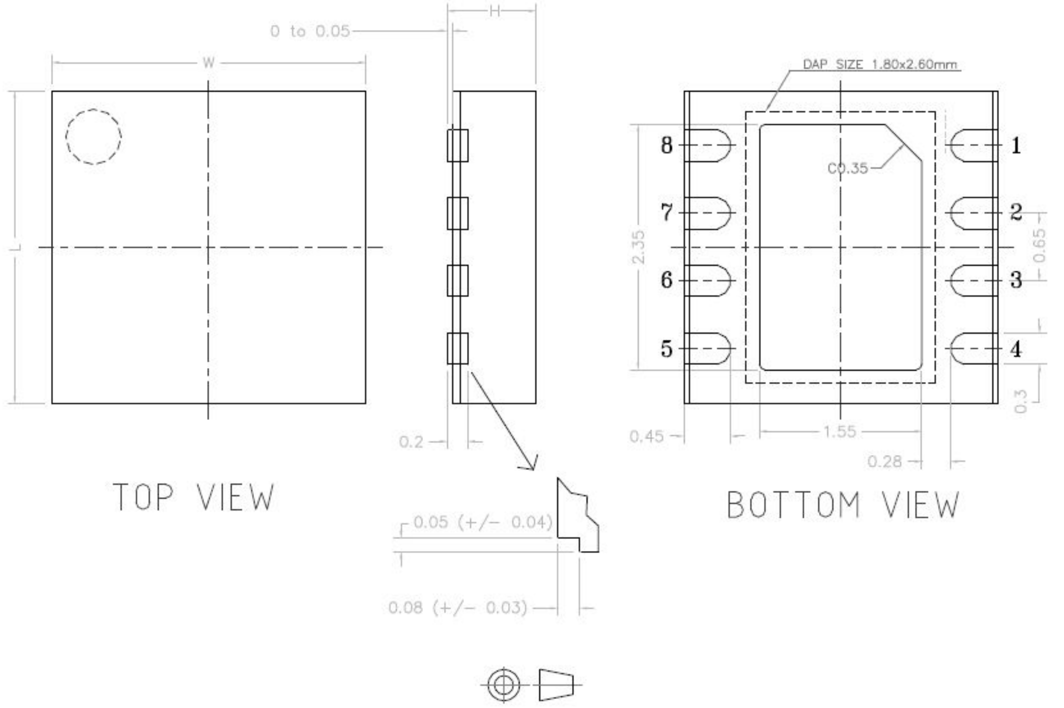


**Table 6: MiniSO8 mechanical data**

| **Ref.** | **Dimensions** | | | | | |
|---|---|---|---|---|---|---|
| | **Millimeters** | | | **Inches** | | |
| | **Min.** | **Typ.** | **Max.** | **Min.** | **Typ.** | **Max.** |
| A | | | 1.1 | | | 0.043 |
| A1 | 0 | | 0.15 | 0 | | 0.006 |
| A2 | 0.75 | 0.85 | 0.95 | 0.030 | 0.033 | 0.037 |
| b | 0.22 | | 0.40 | 0.009 | | 0.016 |
| c | 0.08 | | 0.23 | 0.003 | | 0.009 |
| D | 2.80 | 3.00 | 3.20 | 0.11 | 0.118 | 0.126 |
| E | 4.65 | 4.90 | 5.15 | 0.183 | 0.193 | 0.203 |
| E1 | 2.80 | 3.00 | 3.10 | 0.11 | 0.118 | 0.122 |
| e | | 0.65 | | | 0.026 | |
| L | 0.40 | 0.60 | 0.80 | 0.016 | 0.024 | 0.031 |
| L1 | | 0.95 | | | 0.037 | |
| L2 | | 0.25 | | | 0.010 | |
| k | 0° | | 8° | 0° | | 8° |
| ccc | | | 0.10 | | | 0.004 |

## 5.2 DFN8 3x3 package information

Figure 39: DFN8 3x3 package outline and mechanical data



Dimensions are in millimeter unless otherwise specified
General Tolerance is +/-0.1mm unless otherwise specified

OUTER DIMENSIONS

| ITEM | DIMENSION [mm] | TOLERANCE [mm] |
|---|---|---|
| Length [L] | 3.00 | ±0.15 |
| Width [W] | 3.00 | ±0.15 |
| Height [H] | 0.75 | ±0.05 |

# 6 Ordering information

**Table 7: Order codes**

| Order code | Temperature range | Package | Packing | Marking |
|---|---|---|---|---|
| TSB572IQ2T | -40 °C to 125 °C | DFN8 3x3 | Tape and reel | K31 |
| TSB572IYQ2T (1) | | | | K32 |
| TSB572IST | | MiniSO8 | | K31 |
| TSB572IYST (1) | | | | K32 |

**Notes:**

(1) Automotive qualification according to AEC-Q100.

# 7 Revision history

Table 8: Document revision history

| Date | Version | Changes |
|---|---|---|
| 12-Oct-2015 | 1 | Initial release |
| 17-Dec-2015 | 2 | *Section 2: "Absolute maximum ratings and operating conditions"*: updated ESD, MM value.<br>*Section 6: "Ordering information"*: removed footnote (1) from order code TSB572IQ2T. |

## IMPORTANT NOTICE – PLEASE READ CAREFULLY